FACULTY OF ENGINEERING & TECHNOLOGY
SCHOOL OF ENGINEERING
FINAL YEAR PROJECT

SIMULATION OF VERTICAL CHANNEL MOSFET

NAME: HARKISHEN SINGH A/L JASBIR SINGH

STUDENT ID: 1000309967 (UCSI)

MAJOR: B. ENG (HONS.) ELECTRICAL & ELECTRONICS

1ST SUPERVISOR: DR. KHEDR M.M ABOHASSAN

2ND SUPERVISOR: MS. RUZITA ABU BAKAR

PROJECT COORDINATOR: DR. KHEDR M.M ABOHASSAN

JANUARY – SEPTEMBER 2005

ABSTRACT

The scaling of integrated circuits to smaller physical dimensions has become a primary activity of advance device development. The double gate (DG) MOSFET appears to be one of the most promising new device architectures for miniaturization below 100nm. This research is a simulation based analysis of the device design and circuit performance for the un-doped double gate (DG) MOSFET in symmetric and asymmetric modes of operation. The simulation has been carried out using a compact, physical sub-threshold and threshold model based on the analytical solution of the two dimensions (2-D) Poisson equation. Dependence of the sub-threshold swing and threshold voltages on the channel length, gate oxide thickness and silicon film thickness has also been investigated. Shrinkage of the device size has been known to cause degradation in device performance due to short channel effects. The issue has been discussed comprehensively and solution to overcome these problems has also been presented. This need for new materials with high-k dielectrics has also been viewed.