



University College Sedaya International



# **SCHOOL OF ENGINEERING**

## **FINAL YEAR ENGINEERING PROJECT**

### **DESIGN AND OPTIMIZATION OF A PROTECTION CIRCUIT FOR ESD IN CMOS CIRCUITS**

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## ABSTRACT

This project will outline the principles of a basic CMOS circuit, a review on the ESD events and a layout of an ESD protection circuit design. This project also reviews the phenomena of ESD and the failures caused by the ESD in the IC industry especially in CMOS technology. The ESD simulation design and optimization will be discussed. Practical ESD protection circuit design and examples will be provided and previous approaches to ESD circuit design are discussed, including design theory and specific design examples. Besides that, protection devices such as resistor, ggNMOS, diode and SCR will be included in the discussion. Several ESD test methods such as Transmission line pulsing (TLP), Human body machine (HBM), Machine model (MM) and CDM will be presented. Dependencies of ESD circuit performance on different parameters of a CMOS technology are discussed.

A design and optimization of an effective protection circuit for CMOS is presented. The design includes the I-V characteristics and ESD withstand level of a circuit given the circuit's layout parameters. Results are given for the circuit experiments run on Pspice software. Results of calibrated simulations are also presented and compared to experiments. Details of the Pspice simulation procedure are provided. The proposed ESD protection circuit is analyzed and demonstrated in graph form. The project concludes with a discussion of future work and issues about ESD in future technologies.